AMENDMENTS TO THE CLAIMS

1. (Canceled)

2. (Currently Amended) A data searching system comprising:

a routing table for storing a plurality of next-hop addresses;

a cache memory storing an IP flow table for storing at least one next-hop address which has been selected from the routing table; and

an address pointer table for storing location information indicating an entry address of each next-hop address stored in the IP flow table and relationship information among entry addresses of next-hop address stored in the IP flow table ~~The data searching system according to claim 1~~, wherein the address pointer table comprises a plurality of memory blocks each having a fixed length on a recording medium, located at consecutive addresses,

each memory block comprising:

a first area for storing an entry address indicating a location of a corresponding piece of data stored in the IP flow table; and

a second area for storing one of a next block address and a bottom-indicating flag, the next block address indicating an address of a memory block storing data following the corresponding piece of data, and the bottom-indicating flag indicating that a current memory block is a bottom of a list.

3. (Currently Amended) The data searching system according to claim 2 [[1]], further comprising:

a controller controlling such that the IP flow table is searched for a desired next-hop address before the routing table and, if a hit is found in the IP flow table, then a found next-hop address is used as a search result, and if no hit is found in the cache memory storing the IP flow table, then the routing table is searched for the desired next-hop address and a found next-hop address is used as a search result and is registered

into the IP flow table, wherein a next-hop address with low retrieved frequency is deleted from the IP flow table according to a predetermined condition and all linked memory blocks related to the deleted piece of data are released into available memory blocks.

4. (Currently Amended) A packet processing system comprising:

a microprocessor;

a routing table;

a cache memory storing an IP flow table which is used to increase search speed for packet forwarding; and

an address pointer table for storing location information indicating an entry address of each piece of data stored in the IP flow table and relationship information among entry addresses of pieces of data stored in the IP flow table, wherein the address pointer table comprises a plurality of memory blocks each having a fixed length on a recording medium, located at consecutive addresses,

each memory block comprising:

a first area for storing an entry address indicating a location of a corresponding piece of data stored in the IP flow table; and

a second area for storing one of a next block address and a bottom-indicating flag, the next block address indicating an address of a memory block storing data following the corresponding piece of data, and the bottom-indicating flag indicating that a current memory block is a bottom of a list.

5. (Canceled).

6. (Currently Amended) The packet processing system according to claim 8 [[5]], wherein the address pointer table is provided in a main memory of the microprocessor.

7. (Currently Amended) The packet processing system according to claim 8 [[5]], wherein the address pointer table is provided in the cache memory.

8. (Currently Amended) A packet processing system comprising:

a microprocessor;

a routing table;

a searcher having a cache memory connected thereto, wherein the cache memory stores a search table to increase search speed for packet forwarding; and

an address pointer table for storing location information indicating an entry address of each piece of data stored in the search table and relationship information among entry addresses of pieces of data stored in the search table ~~The packet processing system according to claim 5~~, wherein the address pointer table comprises a plurality of memory blocks each having a fixed length on a recording medium, located at consecutive addresses,

each of the memory blocks comprises:

a first area for storing an entry address indicating a location of a corresponding piece of data stored in the search table; and

a second area for storing one of a next block address and a bottom-indicating flag, the next block address indicating an address of a memory block storing data following the corresponding piece of data, and the bottom-indicating flag indicating that a current memory block is a bottom of a list.

9. (Currently Amended) A control method for controlling a packet processing system comprising:

a microprocessor;

a routing table;

a searcher having a cache memory connected thereto, wherein the cache memory stores a search table to increase in search speed for packet forwarding; and

an address pointer table for storing location information indicating an entry address of each piece of data stored in the search table and relationship information among entry addresses of pieces of data stored in the search table,

the control method comprising:

a) when the routing table has been updated, accessing the address pointer table based on contents of an entry to be changed to obtain location information of the entry to be changed and entries related to the entry to be changed in the cache memory; and

b) changing the entry and related entries so as to be consistent with the routing table,

wherein the address pointer table comprises a plurality of memory blocks each having a fixed length on a recording medium, located at consecutive addresses,

each memory block comprising:

a first area for storing an entry address indicating a location of a corresponding piece of data stored in the IP flow table; and

a second area for storing one of a next block address and a bottom-indicating flag, the next block address indicating an address of a memory block storing data following the corresponding piece of data, and the bottom-indicating flag indicating that a current memory block is a bottom of a list.

10. (Previously Presented) A system comprising:

a first memory for retrievably storing a plurality of next-hop address entries;

a cache memory for storing a copy of a next-hop address entry that has been retrieved from the first memory to retrievably store a plurality of retrieved next-hop address entries;

a second memory for storing a list of retrieved next-hop address entries which are linked from a leading one to a bottom one; and

a data controller for accessing a desired retrieved next-hop address entry by referring to the list stored in the ~~third~~ second memory.

11. (Previously Presented) The system according to claim 10, wherein the data controller processes the desired retrieved next-hop address entry so as to be consistent with a corresponding next-hop address entry stored in the first memory when the corresponding next-hop address entry has been processed.

12. (Previously Presented) The system according to claim 10, wherein each of the next-hop address entries stored in the first memory has a first indicator and a second indicator, the first indicator indicating which one of a single entry and an aggregated entry the entry relates to, wherein the aggregated entry has a plurality of single entries belonging thereto, and the second indicator indicating a leading address of the list in the third memory.

13. (Previously Presented) The system according to claim 10, wherein the list of retrieved next-hop address entries comprises a plurality of memory blocks each corresponding to the retrieved entries, the memory blocks comprising an address of a corresponding retrieved entry in the cache memory and a next pointer indicating one of an address of a next memory block following the memory block and an address of the memory block itself.

14. (Previously Presented) The system according to claim 12, wherein, when an aggregated entry stored in the first memory is designated, the data controller accesses the second memory depending on the second indicator of the aggregated entry to trace the list of single entries related to the aggregated entry so as to access the single entries related to the aggregated entry.

15. (Original) The system according to claim 14, wherein, when contents of the first memory have been updated, the data controller processes the single entries

related to the aggregated entry so as to be consistent with the contents of the first memory.

16. (Previously Presented) A packet switching system comprising:

a routing table for retrievably storing a plurality of routing entries;

a cache memory for storing a flow table having a copy of a routing entry indicating a packet flow that has been retrieved from the routing table to retrievably store a plurality of retrieved packet flows;

an address pointer table for storing a list of retrieved packet flows which are linked from a leading one to a bottom one;

a search processor for accessing a desired retrieved packet flow in the flow table by referring to the list stored in the address pointer table; and

a microprocessor performing a packet routing control.

17. (Original) The packet switching system according to claim 16, wherein, when a routing entry has been designated to be processed according to predetermined routing processing, the search processor processes a corresponding retrieved packet flow in the flow table so as to be consistent with the designated routing entry stored in the routing table.

18. (Previously Presented) The packet switching system according to claim 16, wherein each of the routing entries stored in the routing table has a first indicator and a second indicator, the first indicator indicating which one of a single packet flow and an aggregated packet flow the routing entry relates to when the aggregated packet flow has a plurality of single packet flows belonging thereto, and the second indicator indicating a leading address of the list in the address pointer table.

19. (Previously Presented) The packet switching system according to claim 16, wherein the list of retrieved packet flows comprises a plurality of memory blocks each corresponding to the retrieved packet flows, the memory blocks comprising

an address of a corresponding retrieved packet flow in the flow table and a next pointer indicating one of an address of a next memory block following the memory block and an address of the memory block itself.

20. (Original) The packet switching system according to claim 18, wherein, when an aggregated routing entry stored in the routing table is designated, the search processor accesses the address pointer table depending on the second indicator of the aggregated routing entry to trace the list of single packet flows related to the aggregated routing entry so as to access the single packet flows related to the aggregated routing entry.

21. (Original) The packet switching system according to claim 20, wherein the search processor processes the single packet flows related to the aggregated routing entry so as to be consistent with the routing table when the routing table has been updated.

22. (Previously Presented) A packet switching method comprising:

a) retrievably storing a plurality of routing entries in a routing table;

b) storing a copy of a routing entry indicating a packet flow that has been retrieved from the routing table to retrievably store a plurality of retrieved packet flows in a cache memory;

c) storing a list of retrieved packet flows which are linked from a leading one to a bottom one in an address pointer table; and

d) accessing a desired retrieved packet flow in the cache memory by referring to the list stored in the address pointer table.

23. (Previously Presented) The packet switching method according to claim 22, wherein the step (d) comprises:

when a packet flow corresponding to a received packet fails to be found in the cache memory, searching the routing table for the packet flow;

registering the found packet flow as a routing result into the cache memory;

determining whether the found packet flow is a micro flow belonging to an aggregated flow;

when the found packet flow is the micro flow, searching the cache memory for a bottom retrieved packet flow of the list corresponding to the aggregated flow;

adding the found packet flow to the bottom retrieved packet flow stored in the cache memory; and

when the found packet flow is not the micro flow, storing an address of the found packet flow in the cache memory into a corresponding routing entry in the routing table.

24. (Previously Presented) The packet switching method according to claim 22, wherein the step (d) comprises:

when an aggregated routing entry has been designated to be deleted, deleting each of the retrieved packet flows included in a list related to the aggregated routing entry from the address pointer table until finding a bottom retrieved packet flow of the list;

releasing a chain of the retrieved packet flows formed in the address pointer table to make them available;

deleting a retrieved packet flow corresponding to the aggregated routing entry from the cache memory; and

deleting the aggregated routing entry from the routing table.